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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,001	TADA, TETSUYA	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/314,833.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1 and 7-9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,710,632. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 (Col. 11, lines 37-47)of the U.S. Patent 6,710,632 recites all of the limitations of claim 1 of the instant application. In particularly, claim 1 of U.S. Patent 6,710,632 recites a drive circuit (Col. 11, lines 37-47) comprising a current output MOS, a drive part, and a clamp circuit as recited in claim 1 of the instant application.

With respect to claims 7-9 of the instant application, claim 1 of the U.S. Patent 6,710,632 discloses all of the limitations of these claims except for the drive part includes a first MOS transistor, wherein the first MOS transistor is a first NMOS transistor; a second NMOS transistor, a first current source, wherein the first current source comprises a first PMOS transistor and a second PMOS transistor; a second current source; a first resistive element and a second resistive element as recited in the claims. However, Figure 7 of the prior art of the U.S.

Patent 6,710,632 discloses a drive part (QP5, QP6, R3, R34, R4, QN7, QN8, INV1) includes a first MOS transistor (QN8), wherein the first MOS transistor is a first NMOS transistor (QN8); a second NMOS transistor (QN7), a first current source (QP5-QP6), wherein the first current source comprises a first PMOS transistor (QP4) and a second PMOS transistor (QP6); a first resistive element (R3) and a second resistive element (R34) for the purpose of limiting punch-through current during switching (Col. 3, lines 6-8) and thus reducing power consumption of the circuitry. Thus, it would have been obvious to one skill in the art to use the specific drive part as in Figure 7 of the U.S. Patent 6,710,632 for the drive circuit of claim 1 of U.S. Patent 6,710,632 for the purpose of reducing power consumption of the circuitry. Thus, this modification meets the limitations of claim 7 of the instant application.

Note that, with respect to claims 8 and 9, the above modification as discussed meets all the limitations of claim 8 of the instant application except for a second current source connected between the source terminal of the first NMOS transistor and a reference potential. However, Figure 6 of the prior art of U.S. Patent 6,710,632 discloses a drive part (all elements in Figure 6 except for the resistor R2 and transistor QN6) including a second current source (IS2) connected between the source terminal of the first NMOS transistor (QN5) and a reference potential (ground) for the purpose of controlling and limiting punch-through current during switching of the circuitry (Col. 2, lines 65-67) and thus controlling and reducing the power consumption of the circuitry. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the above combination by providing the drive circuit in Figure 7 of U.S. Patent 6,710,632 with a second current source (IS2) connected between the source terminal of the fourth NMOS transistor and ground, as taught in Figure 6 of the U.S. Patent

6,710,632, for the purpose of reducing and controlling the power consumption of the circuitry. Thus, the limitations of claims 8 and 9 of the instant applicant are also met.

Claim Objections

3. Claim 9 is objected to because of the following informalities: on line 4 of claim 9, "a second resistive terminal" should be changed to --a second resistive element--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yokosawa (USP 6,294,941).

With respect to claim 1, Figure 1 of the Yokosawa reference discloses a drive circuit to supply drive current to a load resistor (9-10) that is connected to first power voltage supply element (52), which includes: a current output MOS transistor (8) connected in series with the load resistor (9-10), a drive part (1) that is connected to a second power voltage supply element (51) and that supplies a drive signal (A) to the gate terminal of the current output MOS transistor (8), and a clamp circuit (28) that is connected to the second power voltage supply terminal (51) to hold the drain terminal of the current output MOS transistor at a predetermined potential (Col. 6, lines 24-40).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Yokosawa (USP 6,294,941).

With respect to claim 1, Figure 7 of the applicant's admitted prior art discloses a drive circuit to supply drive current to a load resistor (R5) that is connected to a first power voltage supply (Vcc2), which includes: a current output MOS transistor (QN9) connected in series with the load resistor, and a drive part (all elements in Figure 7 except for the resistor R5 and transistor QN9) that is connected to a second power supply voltage (Vcc1 or ground) and that supplies a drive signal (ND3) to the gate terminal of the current output MOS transistor. Figure 7 of the applicant's admitted prior art does not disclose that the drive circuit including a clamp circuit that is connected to the second power voltage supply terminal to hold the drain terminal of the current output MOS transistor at a predetermined potential. However, the Yokosawa reference discloses in Figure 1 a circuit that including a clamp circuit (28) for the purpose of limiting the gate-source voltage of the output MOS transistor so as to prevent it from exceeding a predetermined voltage level (Col. 6, lines 29-40). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to provide the drive circuit in Figure 7 of the applicant's admitted prior art with the clamp circuit 28 in Figure 1 of the Yokosawa reference for the purpose of limiting the gate-source voltage of the output MOS transistor so as

to prevent it from exceeding a predetermined voltage level (Col. 6, lines 29-40). Thus, this combination meets all the limitations of claim 1.

With respect to claim 7, Figure 7 of the applicant's admitted prior art in the above modification shows that the drive part includes a first MOS transistor (first NMOS QN8) connected to the gate terminal of the current output MOS transistor (QN9) and that supplies the drive signal to the current output MOS transistor, and a first current source (current mirror QP5-QP6) that supplies current to the first MOS transistor (first NMOS QN8).

With respect to claim 8, the above combination as discussed above meets all the limitation of this claim except for the drive part including a third current source is connected between the source terminal of the first NMOS transistor (QN8) and the reference potential ground. However, Figure 6 of applicant's admitted prior art discloses a drive part (all elements in Figure 6 except for the resistor R2 and transistor QN6) including a second current source (IS2) connected between the source terminal of the first NMOS transistor (QN5) and ground for the purpose of controlling the limiting punch-through current during switching of the circuitry (see lines 22-23 on page 4 of the instant specification) and thus controlling and reducing the power consumption of the circuitry. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the above combination/modification by providing the drive circuit in Figure 7 of the applicant's admitted prior art with a second current source connected between the source terminal of the first NMOS transistor (QN8) and ground, as taught in Figure 6 of the applicant's admitted prior art, for the purpose of limiting punch-through current during switching of the circuitry and thus reducing the power consumption of the circuitry, i.e., connecting a second current source between the source terminal of the first NMOS

(QN8) transistor and ground (GND) in Figure 7 of the applicant's admitted prior art. Thus this modification meets all the limitation of claim 8 because the modification now discloses a circuit wherein the drive part now including: a second current source (IS2 as modified as discussed) that is connected between the source terminal and the reference potential of the first MOS transistor (first NMOS QN8), and a second NMOS transistor (QN7) that is connected between the second current source (QP5-QP6) and the reference potential (GND) and that operates complementarily with the first NMOS transistor (QN8), and the first current source (QP5-QP6) includes a first PMOS transistor (QP5) that is connected between the second power supply voltage terminal and the second NMOS transistor (QN7) and whose gate terminal and drain terminal are connected together, and a second PMOS (QP6) transistor that is connected between the second power supply terminal and a common connection point (ND3) between the gate terminal of the current output MOS transistor and the first NMOS transistor (QN8) , and whose gate terminal is connected to the gate terminal of the first PMOS transistor.

With respect to claim 9, Figure 7 of the applicant's admitted prior art in the above modification shows that the drive part has a first resistive element (R3) that is connected between the drain terminal of the first PMOS transistor and the drain terminal of the second NMOS transistor, and a second resistance element (the resistor connected to the current mirror with transistor QP5) that is connected between the second power supply voltage terminal and the gate terminal of the first PMOS transistor.

Response to Arguments

8. Applicant's arguments filed on 3/10/06 have been fully considered but they are not persuasive.

With regard to the double patenting, applicant argues that the two applications have the same filing date so it is not possible to extend in monopoly since both should have expire on the same date. However, this argument is not persuasive because, according to MPEP, the same expiration date of the two applications is not the basis to withdrawn the double patenting rejection. Note that, in order to overcome the double patenting rejection, applicant needs to file a proper Terminal Disclaimer.

Applicant argues that Yokosawa does not discloses that the clamp circuit to hold the drain terminal of the current output transistor at a predetermined potential. However, this argument is not persuasive because clearly that the clamp circuit 28 of Yokosawa clamps the gate potential of the source follower transistor 8 so that the gate to source of the transistor 8 is hold to a first predetermined potential (Col. 6, lines 24-40) to bias the gate of transistor 8, so the turn-on resistance of the transistor 8 is a predetermined value, and thus the drain terminal of the transistor is hold at a second predetermined potential. Furthermore, in operation of the circuitry of Figure 1 of Yokosawa, the reference potential Vref is a fixed voltage, and when the power supply VBATT is fixed then the circuit of Figure 1 is generated a constant voltage at the output Vout (drain of transistor 8).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER